REMARKS

Upon entry of the instant Amendment, Claims 1-10, 12, 14, and 19-20 are pending. Claims 1, 5, 12, 14, and 19 have been amended to more particularly point out Applicants' invention.

Claims 1, 5, 12, 14, and 19 were objected to because the preambles were indicated to be too general. The preambles of the various claims have been amended to provide greater specificity. As such, Applicants respectfully submit that the basis for the objection is obviated.

Claims 1-10, 12, 14, and 16-20 have been rejected under 35 U.S.C. 103 as being unpatentable over Paradine et al., U.S. Patent No. 6,049,565 ("Paradine") in view of Hirata, U.S. Patent No. 5,327,391 ("Hirata"). Applicants respectfully submit that the claimed invention is not taught, suggested or implied by Hirata or Paradine, either singly or in combination.

As discussed in the Specification, the present invention relates to a system and method for rate adjustment. A rate adjustment system according to an embodiment of the invention includes a first jitter buffer pair and a second buffer pair. The buffers in the first and second jitter buffer pairs are swapped to effect a rate adjustment. In particular, the buffers in the pairs are alternately filled at a first clock rate and emptied at a second. The swapping occurs simultaneously at the second clock rate. In some embodiments, the first cock is associated with a sample clock frequency and the second clock is associated with a frame clock frequency.

Thus, claim 1 has been amended to recite "said first clocking frequency associated with a sample clock, said second clocking frequency associated with a frame clock;" claim 5 has been amended to recite "said first clock frequency associated with a sample clock, said second clock frequency associated with a frame clock;" claim 12 has been amended to recite "said first clock rate being associated with a sample clock, said second clock rate being associated with a frame clock;" claim 14 has been amended to recite "said first clock rate being a sample clock rate, said second clock rate being a frame clock rate;" and claim 19 has been amended to recite "wherein ones

of said pairs of first or second jitter buffers are swapped simultaneously according to a clock by which said ones of said pairs of first or second jitter buffers are filled or emptied, said clock comprising a frame clock rate."

In contrast, as discussed in response to the previous Official Action, and contrary to the suggestion in the Official Action, neither reference relates to simultaneously swapping pairs of buffers as generally recited in the claims at issue. Further, neither reference provides that a first clock frequency is associated with a sample clock and a second is associated with a frame clock, as generally recited in the claims at issue.

As an initial matter, Applicants note that Paragraph 4 of the Official Action appears to suggest that Paradine is not relied on to show alternation or swapping of the buffers.

However, Applicants note that Paragraph 3 of the Official Action, at page 3, reproduced below, states

> Paradine et al teach. . .
> Wherein the first or second jitter buffers (320 double buffer for audio IN path) alternately fill at a first clock frequency (sampling clock via 305 CODEC circuitry block) and empty at a second clock frequency *(clock on DSP side for network interface)(See Col. 4, lines 27-50),
> Wherein alternation between the first and second jitter buffers occurs at the second clock frequency (CCITT G.711 format 8 ms frame for DSP/network interface, See Col. 5, lines 55-65).

Thus it is unclear to Applicants what precisely Paradine is being relied upon to teach (i.e., alternation or swapping of double buffers; or the mere existence in the art of double buffers?). If Paradine is not being relied upon to allegedly teach alternation, Applicants agree that Paradine does not, in fact, teach, suggest, or imply, inter alia, such limitations. However, if Paradine is being relied upon to teach alternation, Applicants respectfully disagree.

As discussed in response to the previous Official Action, while Paradine provides a double buffer 320 and a double buffer 330, the halves of the double buffers are never alternated or swapped. Instead, samples are passed into one half of the buffer and read out of the other. No swapping of halves occurs.

Applicants respectfully submit that Hirata similarly fails to disclose simultaneously switching individual ones of pairs of buffers according to a same (frame)

frequency, as generally recited in the claims at issue. As discussed above, according to embodiments of the present invention, one pair of buffers operates in a first "direction" and the other operates in a second "direction." That is, the first pair is filled at a first clock and emptied at a second clock rate. The second pair is filled at the second clock rate and emptied at the first. The individual buffers in the pairs are simultaneously swapped at the second clock rate. Thus, both oppositely directed pairs are swapped according to the same clock rate. In some embodiments, the rate at which the buffers are swapped is a frame clock rate.

In contrast, Hirata provides a first data memory 24-1 and a second data memory 24-2. Usage of the first and second data memories is governed by selector 23. First generating circuit 21 provides input to write in counters 25-1 and 25-2 and second signal generating circuit provides input to read-out counters 26-1 and 26-2. Nevertheless, Hirata nowhere provides for oppositely directed pairs of jitter buffers to be simultaneously swapped at a common frame clock rate. Hirata is merely unidirectional. Thus, even if combined with Paradine, the result would be different selectors operating in different clock domains, which could not achieve the simultaneous swapping or alternation as generally recited in the claims at issue. That is, the selection of buffers would be done at different clocks, as opposed to the present invention, in which swapping occurs at a same clock rate. Furthermore, Hirata provides two frame clock rates 102, 104, which are each derived from different sources, rather than a single frame clock as generally recited in the claims at issue. Thus, Hirata does not provide for swapping pairs of buffers at the common frame clock rate.

As such, the Examiner is respectfully requested to reconsider and withdraw the rejection of the claims.

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For all of the above reasons, Applicants respectfully submit that the application is in condition for allowance, which allowance is earnestly solicited.

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